One of the most exciting developments in science and engineering over the past few years has been the progress toward architectures, materials, and devices for nanoscale and molecular-electronics-based computing systems. These progresses met the need of the microelectronics industry for ever increasing performances and small feature sizes. NASIC(5) is one example of such architecture. They are based on a variety of nanodevices but still require some supporting CMOS circuitry. The manufacturing process of these fabrics proposes a combination of lithographic processes and bottom-up self assembly, thus imposing some constraints on the architecture layout and reliability. The regularity of assembly and the huge number of faults are mainly the principal effects of the bottom-up self assembly.

Based upon our experience with the FPGA CAD framework Madeo(2), we introduced NANO MADEO(1): a generic, evolutive CAD framework for automatic circuit layout. The principal characteristics of this framework is its capacity to explore the complex solution space circuits/architectures/algorithms/metrics, enabling three principal prospection possibilities using different metrics. Here, we are presenting NABOO a prototype implementation of the physical design steps in NANO MADEO.

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**Architectural Model**

Parametric virtual representation of the nanofabrics, encapsulates the topological and physical constraints of the target architecture. Principal characteristics:

1. Nano/CMOS device representation: FET, nanowire, microwire, etc.;
2. Basic architectural primitives: crossbar, nanotile, etc.;
3. Hierarchical composition of 1 and 2;
   -- Integrates new hybrid architectures through model evolution;
   -- Enables reconfigurable and non-reconfigurable fabric modeling;
   -- Offers the architectural support for the physical layout tools.

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**Structured Circuit Model**

Polymorphic model capturing the structural characteristics of a circuit. Principal characteristics:

1. Encapsulate behavioral code, memory elements, etc.;
2. Hierarchical circuit representations based on composites and aliasing;
   -- Powerful tools (circuit simulation and visual editing) inherited from Madeo.

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**Physical Layout Tools**

Generic, modular, pluggable set of tools built around the circuit and architectural models.

The open framework model enables the possibility of highly specialized tools to coexist with the general purpose one.

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**Conclusions and Future work**

The evolution of the computing architectures forces also the evolution of CAD tools. In the context of nanofabrics the tools must be able to cope with a huge number of relatively regular structures, they should integrate support for: 1. fault tolerance, 2. nano/CMOS application partitioning.

The preliminary NABOO implementation proved the viability of a MDA-based generic framework targeting application physical design automation on nanofabrics. NABOO, in the future:

- Rich set of generic tools for physical design;
- Integration of defect maps and other defect tolerance techniques;
- Extended architectural support for nanofabrics (architectural modeling and tool support);

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**References**


