In turbo decoding of product codes, we propose a novel algorithm, based on the Chase-Pyndiah algorithm, which exhibits a modular, simple structure with fine grain parallelism. It is implemented into deep pipelined architectures, including an interleaving block decoding scheme, with good potential on FPGAs and MP-SoCs targets. We include an evaluation of the essential parameters of those architectures, which are situated in a different area of the block turbo decoder design space.


devoted to the ValMadeo project.

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Conclusions and Future work

Implementation of Mini-Maxi algorithm inspired from Chase-Pyndiah algorithm.

Hardware constraints based synthesis.

• prototype of the interleaved decoder architecture on a Celoxica development board (RC10, RC20x).

• MPSoC implementation

• IP integration into Nomadik platform

References


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